REMARKS

In order to place the instant application in better condition for allowance, the title, specification and abstract have been amended for improved clarity and definiteness, and to more accurately describe the instant invention. Thus, for example, the description of the figure has been amended in order to more precisely describe that the control semiconductor chip 40 employs bulk technology as opposed to SOI technology, with no insulating layer between device 42 and substrate 46, as is clearly shown and disclosed in the figure, and in contrast to SOI device 30 which is clearly shown and described as comprising an insulation layer 39. Additionally, the relationship between the power and control chips is clarified, in the sense that the power chip pertains to a chip which may contain an output circuit or the like which operates at a higher power level than that of the control chip, and that no specific power level is to be implied. In this regard, it is noted that the original specification did not limit the power semiconductor chip to any specific power level.

On the merits, claims 1-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Takagi et al in view of the admitted prior art, for the reasons of record. In response, claim 8 has been canceled, without prejudice, and claim 1 has been amended in order to more precisely define the instant invention.

It is respectfully submitted that the currently-pending claims, as herein amended, are now clearly patentably distinguishable over the cited and applied art for the reasons detailed below.

As noted in the instant specification, the admitted prior art relates to a complicated and uneconomical structure, in which a chip is provided on an electrode plate, which is in turn provided on an insulating ceramic plate provided on the heat sink. Such a configuration is not only complicated and uneconomical, but may also be subject to EMI radiation.

The cited structure (Fig. 12) in Takagi relates to a device in which both the power and control semiconductor chips employ SOI technology, with an insulating layer (10, 80) present between the active circuitry and the subject of both chips. Absent the benefit of impermissible hindsight derived from the instant disclosure, this would be the logical and expected way to provide multiple chips on a single conductive substrate.

In the present invention, on the contrary, the power and control semiconductor chips employ different technologies, with the power chip being fabricated in SOI technology and the control chip being fabricated in bulk technology, without an insulating layer, as clearly shown in the Figure. In order to more clearly and precisely recite this distinction claim 1 has been amended in order to more specifically recite that the control semiconductor chip

comprises a bulk technology semiconductor device. It is respectfully submitted that claim 1, and the remaining claims depending therefrom, now define an invention which is neither shown nor suggested by the two substantially different technologies shown in the two cited and applied references, and that the currently-pending claims, as herein amended, are clearly patentably distinguishable over the cited prior art. Allowance of the currently-pending claims is therefore respectfully submitted to be justified, and favorable consideration is earnestly solicited.

Respectfully submitted,

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APPENDIX A

Amended Specification

Page 1, in the paragraph beginning on line 1, change as follows:

The invention is in the field of semiconductor devices, and relates more specifically to multiple semiconductor chip (hereinafter multi-chip) modules for use ~~high-power~~ in power applications.

Page 2, in the paragraph beginning on line 7, change as follows:

Accordingly, it would be desirable to have a multi-chip module for use in ~~high~~ power applications which is simple in construction and therefore economical to fabricate, and in which performance parameters such as reduced EMI are enhanced.

Page 2, in the paragraph beginning on line 13, change as follows:

It is therefore an object of the present invention to provide a multi-chip module for use in ~~high~~ power applications which is simple in construction, economical to fabricate, and capable of offering enhanced performance.

Page 3, in the paragraph beginning on line 25, change as follows:

In the simplified cross-sectional view of the single Figure, a multiple semiconductor chip (multi-chip) module 10 for use in ~~high-~~ power circuit applications is shown. The multi-chip module 10 includes an electrically conductive heat sink 20, typically a metal heat sink of copper or aluminum, on which are directly mounted a plurality of semiconductor chips, such as chips 30 and 40 shown in simplified form within bold rectangles in the Figure. It should be noted that the semiconductor chips 30 and 40 are directly mounted on the conductive heat sink 20 without the use of a separate electrical insulation layer as is typically required in the prior art.

Page 4, in the paragraph beginning on line 10, change as follows:

In the example shown, semiconductor chip 30 is a power semiconductor chip, here shown as a Silicon-On-Insulator (SOI) device having a semiconductor substrate 38, a buried insulating layer 39, and an SOI layer 32 having at least one semiconductor device symbolically shown by region 34 provided therein. The term "power semiconductor chip" is to be understood as relating to any chip, such as a chip containing an output circuit, which operates at a higher power level than that of the control chip, and not to any specific power level. Electrical connections to the semiconductor device 34 are symbolically shown by the single

electrode 36, although it will be apparent that in an actual device more than one connection will typically be provided. By placing all of the relatively high-voltage and high-power components of the multi-chip module on SOI power semiconductor chip 30, it becomes possible to directly mount the semiconductor chip on the conductive heat sink 20 without the use of a separate electrical insulation layer, since the portions of the chip connected to high voltage are insulated from the substrate 38 by oxide insulation layer ~~36~~ 39 within the chip itself. Power semiconductor chip 30 can be directly mounted on the conductive heat sink 20 by known conventional methods, such as soldering or gluing with a conductive glue. If power semiconductor chips other than SOI chips are used, they must be capable of operating with their substrates connected directly to the conductive heat sink.

Page 5, in the paragraph beginning on line 4, change as follows:

The multi-chip module 10 also includes a control semiconductor chip 40 shown in simplified form in the Figure, also directly mounted on the conductive heat sink 20 without the use of a separate electrical insulation layer. The control semiconductor chip 40 is symbolically shown by a substrate 46 in which is formed at least one semiconductor device 42, with electrical connections to the device being symbolically shown by the single connection

electrode 44. As shown in the Figures, control semiconductor chip 40 employs bulk technology as opposed to SOI technology, with no insulating layer between device 42 and substrate 46.

Page 6, in the paragraph beginning on line 21, change as follows:

In the foregoing manner, the present invention provides a multi-chip module for use in ~~high~~-power applications which is simple in structure, economical to fabricate and which offers performance advantages.

APPENDIX B

Amended Claim

1. (amended) A multiple semiconductor chip (multi-chip) module ~~for use in high-power applications~~, comprising at least a power semiconductor chip and a control semiconductor chip mounted on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor chip comprises a bulk technology semiconductor device having a substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer.

ABSTRACT OF THE DISCLOSURE

A multiple semiconductor chip (multi-chip) module for use in power applications includes at least a power semiconductor chip and a control semiconductor chip mounted on an electrically conductive heat sink. The power semiconductor chip may be a Silicon-On-Insulator (SOI) device and the control semiconductor chip may be a semiconductor device having a substrate connected to ground potential. The power semiconductor chip and the control semiconductor chip are directly mounted on the electrically conductive heat sink without the use of a separate electrical insulation layer in order to obtain a multi-chip module which is simple and economical to manufacture, and which offers superior performance characteristics.